REMARKS

This is a full and timely response to the outstanding Non-Final Office Action mailed July 7, 2009. Upon entry of the amendments in this response, claims 1 – 20 remain pending. In particular, Applicants amend claim 8. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Initial Matters

Applicants first note that this is the sixth (6^{th}) consecutive Non-Final Office Action issued in the present application. Additionally, the Examiner performed a new search for each of the six (6) Non-Final Office Actions. (See PAIR Image File Wrapper on 01/29/07, 05/29/07, 12/26/07, 07/14/08, 01/14/09, 07/07/09). However, the Examiner has yet to find any art that may be used to adequately reject any of the pending claims.

Applicants respectfully submit that multiple piecemeal searches, as performed in the present application, violates MPEP §904, which states "[t]he first search should be such that the examiner need not ordinarily make a second search of the prior art, unless necessitated by amendments to the claims by the applicant in the first reply." Additionally, as the Examiner has been unable to find any art in any of the six (6) searches that discloses, teaches, or suggest all of the claimed elements, Applicants submit an allowance of the present application should be forthcoming.

II. Examiner Interview

Applicants wish to express their sincere appreciation for the time that Examiner Chan spent with Applicants' Attorney, Anthony Bonner, during a telephone discussion on September 15, 2009 regarding the outstanding Office Action. During that conversation, Examiner Chan and Mr. Bonner discussed potential arguments and amendments with regard to claim 1, in view of

Gaytan. Thus, Applicants respectfully request that Examiner Chan carefully consider this response.

III. Rejections Under 35 U.S.C. §103

A. Claim 1 is Allowable Over *Gaytan, Priem,* and *Beshi*

The Office Action indicates that claim 1 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 5,638,367 ("*Gaytan*"), in view of U.S. Patent Number 6,023,738 ("*Priem*"), and further in view of U.S. Publication Number 20040213291 ("*Beshi*"). Applicants respectfully traverse this rejection for at least the reason that *Gaytan* in view of *Priem* and *Beshi* fails to disclose, teach, or suggest all of the elements of claim 1. More specifically, claim 1 recites:

> A method for transferring network packet data that is stored in memory to an output device, the method comprising the steps of:
>
> concatenating one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word;
>
> storing the first sequence of packet data octets in a FIFO buffer operably connected to the output device when the octet length of the sequence of packet data octets is equal to the octet length of a data word; and
>
> storing a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and ***storing a remaining second subset of packet data octets from the first sequence in an alignment register*** when the octet length of the first sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word.
>
> ***(Emphasis added).***

Applicants respectfully submit that claim 1 is allowable for at least the reason that none of *Gaytan*, *Priem*, and *Beshi*, taken alone or in combination, discloses, teaches, or suggests a "method for transferring network packet data that is stored in memory to an output device, the method comprising the steps of… storing a first subset of packet data octets from the first

sequence of packet data octets in the FIFO buffer and ***storing a remaining second subset of packet data octets from the first sequence in an alignment register*** when the octet length of the first sequence of packet data octets exceeds the octet length of a data word, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word" as recited in claim 1. More specifically, *Gaytan* discloses "one primary function of the System and ATM Layer Core 220 is to retrieve data from host memory and to perform packing operations on the data before temporarily storing the data within the TX buffer memory through packing circuitry… Thereafter, the data may be segmented into cells and transferred to the array of TX FIFOs" (column 5, line 52). As illustrated in this passage, *Gaytan* does not disclose "***storing a remaining second subset of packet data octets from the first sequence in an alignment register*** when the octet length of the first sequence of packet data octets exceeds the octet length of a data word" as recited in claim 1.

Additionally, *Priem* fails to overcome the deficiencies of *Gaytan*. More specifically, *Priem* discloses "[s]pace is also provided for overflows which do occur to eliminate any chance of data loss" (column 4, line 5). As illustrated in this passage, *Priem* discloses that if a FIFO runs out of space, the "overflow component" (FIG. 1) may be configured to receive the overflow data. However, nowhere is there any suggestion that the "overflow component" in *Priem* is "an alignment register" as recited in claim 1. Further, not withstanding this fact, as *Priem* merely discloses sending overflow data to the "overflow component," there is no suggestion in *Priem* that the data is stored in the "overflow component" "when the octet length of the first sequence of packet data octets exceeds the octet length of a data word" as recited in claim 1. More specifically, simple overflow is not enough to render claim 1 obvious.

Further, *Beshi* fails to overcome the deficiencies of *Gaytan* and *Priem*. More specifically, *Beshi* discloses "stor[ing] fractional segments (null-padded) that are either awaiting concatenation with a forthcoming segment of the same data stream, or awaiting transfer

permission despite the null-padding if a quality-control count recorded in a corresponding field 912 reaches a threshold" (page 8, paragraph [0089]). However, *Beshi* fails to even suggest "***storing a remaining second subset of packet data octets from the first sequence in an alignment register*** when the octet length of the first sequence of packet data octets exceeds the octet length of a data word" as recited in claim 1. For at least these reasons, claim 1 is allowable.

B. Claim 2 is Allowable Over *Gaytan*, *Priem*, and *Beshi*

The Office Action indicates that claim 2 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 5,638,367 ("*Gaytan*"), in view of U.S. Patent Number 6,023,738 ("*Priem*"), and further in view of U.S. Publication Number 20040213291 ("*Beshi*"). Applicants respectfully traverse this rejection for at least the reason that *Gaytan* in view of *Priem* and *Beshi* fails to disclose, teach, or suggest all of the elements of claim 2. More specifically, the Office Action argues "Gaytan et al. clearly show the step of storing the first sequence of packet data octets in the alignment register (FIG. 6a (63), col. 7, lines 21-31 (64-bit data word)) when the octet length of the first sequence of packet data octets is less than the octet length of a data word (FIG. 6a (63), col. 7, lines 21-31 (64-bit data word))" (OA page 4, last paragraph). Applicants respectfully disagree. On the lines cited by the Office Action, *Gaytan* discloses:

> Referring now to FIG. 6b, the byte packing circuit 650 comprises a byte rotate circuit 655, an input storage element 660, a save storage element 665, an output storage element 670 and a selector 675. The input storage element 660 receives Data[31:0] from the word packing circuit 660 and routes Data [31:0] to both the save storage element 665 and the selector 675. The save storage element 665 delays Data[31:0] by a single cycle and outputs the data (referred to as 'SData[31:0]') into the selector 675. Thus, the selector 670 receives data input from both the input storage element 660 and the save storage element 665.

(Column 7, lines 21 – 31).

As illustrated in this passage, *Gaytan* fails to even suggest "storing the first sequence of packet data octets in the alignment register ***when the octet length of the first sequence of packet data octets is less than the octet length of a data word***" (***emphasis added***) as recited in claim 2.

Further, not withstanding this fact, *Priem* clearly teaches away from this element. More specifically, as discussed above, *Priem* discloses that data is first input into a FIFO and, when the FIFO is full, the overflow data is sent to an "overflow component." However, claim 2 teaches that the first sequence of packet data octets (the data that the Office Action argues is sent to the FIFO and not the "overflow component") is sent to the alignment register "***when the octet length of the first sequence of packet data octets is less than the octet length of a data word***." *Priem* clearly teaches away from this because the data in *Priem* always first goes to the FIFO. Only when the data in the FIFO overflows, is the data sent to the "overflow component." Consequently, a combination that includes *Priem* cannot disclose "storing the first sequence of packet data octets in the alignment register ***when the octet length of the first sequence of packet data octets is less than the octet length of a data word***" (***emphasis added***) as recited in claim 2. For at least these reasons, claim 2 is allowable.

C. Claim 5 is Allowable Over *Gaytan*, *Priem*, and *Beshi*

The Office Action indicates that claim 5 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 5,638,367 ("*Gaytan*"), in view of U.S. Patent Number 6,023,738 ("*Priem*"), and further in view of U.S. Publication Number 20040213291 ("*Beshi*"). Applicants respectfully traverse this rejection for at least the reason that *Gaytan* in view of *Priem* and *Beshi* fails to disclose, teach, or suggest all of the elements of claim 5. More specifically, claim 5 recites:

> A system for transferring network packet data stored in memory to an output device, the system comprising:
>
> a direct memory access (DMA) interface for accessing a set of data words stored in memory, each data word having at least one valid octet to be included in a network packet and each data word being accessed using a DMA address associated with the data word;
>
> a first in-first out (FIFO) buffer for storing network packet data to be transmitted by the output device; and
>
> an alignment block having at least one alignment register, wherein the alignment register for storing at least one data octet, and wherein the alignment block is adapted to:
>
> concatenate one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word;
>
> store the first sequence of packet data octets in a FIFO buffer operably connected to the output device when the octet length of the sequence of packet data octets is equal to the octet length of a data word; and
>
> store a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and ***store a remaining second subset of packet data octets from the first sequence in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word***, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word.
>
> ***(Emphasis added).***

Applicants respectfully submit that claim 5 is allowable for at least the reason that none of *Gaytan*, *Priem*, and *Beshi*, taken alone or in combination, discloses, teaches, or suggests a "system for transferring network packet data stored in memory to an output device, the system comprising… an alignment block… adapted to… store a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and storing a remaining second subset of packet data octets from the first sequence in an alignment register ***when the octet length of the first sequence of packet data octets exceeds the octet length of a data word***, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word" as recited in claim 5. More specifically, *Gaytan* discloses "one primary function of the System and ATM Layer Core 220 is to retrieve data from host memory and to

perform packing operations on the data before temporarily storing the data within the TX buffer memory through packing circuitry… Thereafter, the data may be segmented into cells and transferred to the array of TX FIFOs" (column 5, line 52). As illustrated in this passage, *Gaytan* does not disclose "***stor[ing] a remaining second subset of packet data octets from the first sequence in an alignment register*** when the octet length of the first sequence of packet data octets exceeds the octet length of a data word" as recited in claim 5.

Additionally, *Priem* fails to overcome the deficiencies of *Gaytan*. More specifically, *Priem* discloses "[s]pace is also provided for overflows which do occur to eliminate any chance of data loss" (column 4, line 5). As illustrated in this passage, *Priem* discloses that if a FIFO runs out of space, the "overflow component" (FIG. 1) may be configured to receive the overflow data. However, nowhere is there any suggestion that the "overflow component" in *Priem* is "an alignment register" as recited in claim 5. Further, not withstanding this fact, as *Priem* merely discloses sending overflow data to the "overflow component," there is no suggestion in *Priem* that the data is stored in the "overflow component" "when the octet length of the first sequence of packet data octets exceeds the octet length of a data word" as recited in claim 5. More specifically, simple overflow is not enough to render claim 5 obvious.

Further, *Beshi* fails to overcome the deficiencies of *Gaytan* and *Priem*. More specifically, *Beshi* discloses "stor[ing] fractional segments (null-padded) that are either awaiting concatenation with a forthcoming segment of the same data stream, or awaiting transfer permission despite the null-padding if a quality-control count recorded in a corresponding field 912 reaches a threshold" (page 8, paragraph [0089]). However, *Beshi* fails to even suggest "***stor[ing] a remaining second subset of packet data octets from the first sequence in an alignment register*** when the octet length of the first sequence of packet data octets exceeds the octet length of a data word" as recited in claim 5. For at least these reasons, claim 5 is allowable.

D. Claim 6 is Allowable Over *Gaytan*, *Priem*, and *Beshi*

The Office Action indicates that claim 6 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 5,638,367 ("*Gaytan*"), in view of U.S. Patent Number 6,023,738 ("*Priem*"), and further in view of U.S. Publication Number 20040213291 ("*Beshi*"). Applicants respectfully traverse this rejection for at least the reason that *Gaytan* in view of *Priem* and *Beshi* fails to disclose, teach, or suggest all of the elements of claim 6. More specifically, the Office Action argues "Gaytan et al. clearly show the step of storing the first sequence of packet data octets in the alignment register (FIG. 6a (63), col. 7, lines 21-31 (64-bit data word)) when the octet length of the first sequence of packet data octets is less than the octet length of a data word (FIG. 6a (63), col. 7, lines 21-31 (64-bit data word))" (OA page 4, last paragraph, referring to claim 2). Applicants respectfully disagree. On the lines cited by the Office Action, *Gaytan* discloses:

> Referring now to FIG. 6b, the byte packing circuit 650 comprises a byte rotate circuit 655, an input storage element 660, a save storage element 665, an output storage element 670 and a selector 675. The input storage element 660 receives Data[31:0] from the word packing circuit 660 and routes Data [31:0] to both the save storage element 665 and the selector 675. The save storage element 665 delays Data[31:0] by a single cycle and outputs the data (referred to as 'SData[31:0]') into the selector 675. Thus, the selector 670 receives data input from both the input storage element 660 and the save storage element 665.

(Column 7, lines 21 – 31).

As illustrated in this passage, *Gaytan* fails to even suggest "stor[ing] the first sequence of packet data octets in the alignment register ***when the octet length of the first sequence of packet data octets is less than the octet length of a data word***" (***emphasis added***) as recited in claim 6.

Further, not withstanding this fact, *Priem* clearly teaches away from this element. More specifically, as discussed above, *Priem* discloses that data is first input into a FIFO and, when

the FIFO is full, the overflow data is sent to an "overflow component." However, claim 6 teaches that the first sequence of packet data octets (the data that the Office Action argues is sent to the FIFO and not the "overflow component") is sent to the alignment register "***when the octet length of the first sequence of packet data octets is less than the octet length of a data word***." *Priem* clearly teaches away from this because the data in *Priem* always first goes to the FIFO. Only when the data in the FIFO overflows, is the data sent to the "overflow component." Consequently, a combination that includes *Priem* cannot disclose "stor[ing] the first sequence of packet data octets in the alignment register ***when the octet length of the first sequence of packet data octets is less than the octet length of a data word***" (***emphasis added***) as recited in claim 6. For at least these reasons, claim 6 is allowable.

E. Claim 14 is Allowable Over *Gaytan, Priem,* and *Beshi*

The Office Action indicates that claim 14 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 5,638,367 ("*Gaytan*"), in view of U.S. Patent Number 6,023,738 ("*Priem*"), and further in view of U.S. Publication Number 20040213291 ("*Beshi*"). Applicants respectfully traverse this rejection for at least the reason that *Gaytan* in view of *Priem* and *Beshi* fails to disclose, teach, or suggest all of the elements of claim 14. More specifically, claim 14 recites:

> A system for transferring network packet data stored in memory to an output device, the method comprising:
>
> means for concatenating one or more packet data octets from at least a first data word having at least one packet data octet to be included in a network packet to generate a first sequence of packet data octets having an octet length at least as great as an octet length of a data word;
>
> means for storing the first sequence of packet data octets in a FIFO buffer operably connected to the output device when the octet length of the sequence of packet data octets is equal to the octet length of a data word; and
>
> means for storing a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and ***storing a remaining second subset of packet data octets from the first sequence in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word***, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word.

(Emphasis added).

Applicants respectfully submit that claim 14 is allowable for at least the reason that none of *Gaytan*, *Priem*, and *Beshi*, taken alone or in combination, discloses, teaches, or suggests a "system for transferring network packet data stored in memory to an output device, the method comprising… means for storing a first subset of packet data octets from the first sequence of packet data octets in the FIFO buffer and ***storing a remaining second subset of packet data octets from the first sequence in an alignment register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word***, wherein an octet length of the first subset of packet data octets is equal to the octet length of a data word" as recited in claim 14. More specifically, *Gaytan* discloses "one primary function of the System and ATM Layer Core 220 is to retrieve data from host memory and to perform packing operations on the data before temporarily storing the data within the TX buffer memory through packing circuitry… Thereafter, the data may be segmented into cells and transferred to the array of TX FIFOs" (column 5, line 52). As illustrated in this passage, *Gaytan* does not disclose "***storing a remaining second subset of packet data octets from the first sequence in an alignment***

register when the octet length of the first sequence of packet data octets exceeds the octet length of a data word" as recited in claim 14.

Additionally, *Priem* fails to overcome the deficiencies of *Gaytan*. More specifically, *Priem* discloses "[s]pace is also provided for overflows which do occur to eliminate any chance of data loss" (column 4, line 5). As illustrated in this passage, *Priem* discloses that if a FIFO runs out of space, the "overflow component" (FIG. 1) may be configured to receive the overflow data. However, nowhere is there any suggestion that the "overflow component" in *Priem* is "an alignment register" as recited in claim 14. Further, not withstanding this fact, as *Priem* merely discloses sending overflow data to the "overflow component," there is no suggestion in *Priem* that the data is stored in the "overflow component" "when the octet length of the first sequence of packet data octets exceeds the octet length of a data word" as recited in claim 14. More specifically, simple overflow is not enough to render claim 14 obvious.

Further, *Beshi* fails to overcome the deficiencies of *Gaytan* and *Priem*. More specifically, *Beshi* discloses "stor[ing] fractional segments (null-padded) that are either awaiting concatenation with a forthcoming segment of the same data stream, or awaiting transfer permission despite the null-padding if a quality-control count recorded in a corresponding field 912 reaches a threshold" (page 8, paragraph [0089]). However, *Beshi* fails to even suggest "***storing a remaining second subset of packet data octets from the first sequence in an alignment register*** when the octet length of the first sequence of packet data octets exceeds the octet length of a data word" as recited in claim 14. For at least these reasons, claim 14 is allowable.

F. Claim 15 is Allowable Over *Gaytan, Priem,* and *Beshi*

The Office Action indicates that claim 15 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 5,638,367 ("*Gaytan*"), in view of U.S. Patent Number 6,023,738 ("*Priem*"), and further in view of U.S. Publication Number 20040213291 ("*Beshi*"). Applicants respectfully traverse this rejection for at least the reason that *Gaytan* in view of *Priem* and *Beshi* fails to disclose, teach, or suggest all of the elements of claim 15. More specifically, the Office Action argues "Gaytan et al. clearly show the step of storing the first sequence of packet data octets in the alignment register (FIG. 6a (63), col. 7, lines 21-31 (64-bit data word)) when the octet length of the first sequence of packet data octets is less than the octet length of a data word (FIG. 6a (63), col. 7, lines 21-31 (64-bit data word))" (OA page 4, last paragraph, referring to claim 2). Applicants respectfully disagree. On the lines cited by the Office Action, *Gaytan* discloses:

> Referring now to FIG. 6b, the byte packing circuit 650 comprises a byte rotate circuit 655, an input storage element 660, a save storage element 665, an output storage element 670 and a selector 675. The input storage element 660 receives Data[31:0] from the word packing circuit 660 and routes Data [31:0] to both the save storage element 665 and the selector 675. The save storage element 665 delays Data[31:0] by a single cycle and outputs the data (referred to as 'SData[31:0]') into the selector 675. Thus, the selector 670 receives data input from both the input storage element 660 and the save storage element 665.

(Column 7, lines 21 – 31).

As illustrated in this passage, *Gaytan* fails to even suggest "storing the first sequence of packet data octets in the alignment register ***when the octet length of the first sequence of packet data octets is less than the octet length of a data word***" (***emphasis added***) as recited in claim 15.

Further, not withstanding this fact, *Priem* clearly teaches away from this element. More specifically, as discussed above, *Priem* discloses that data is first input into a FIFO and, when the FIFO is full, the overflow data is sent to an "overflow component." However, claim 15

teaches that the first sequence of packet data octets (the data that the Office Action argues is sent to the FIFO and not the "overflow component") is sent to the alignment register "***when the octet length of the first sequence of packet data octets is less than the octet length of a data word***." *Priem* clearly teaches away from this because the data in *Priem* always first goes to the FIFO. Only when the data in the FIFO overflows, is the data sent to the "overflow component." Consequently, a combination that includes *Priem* cannot disclose "stor[ing] the first sequence of packet data octets in the alignment register ***when the octet length of the first sequence of packet data octets is less than the octet length of a data word***" (***emphasis added***) as recited in claim 15. For at least these reasons, claim 15 is allowable.

G. Claims 2 – 4, 6 – 13, and 15 – 20 are Allowable Over *Gaytan, Priem,* and *Beshi*

The Office Action indicates that claims 2 – 4, 6 – 13, and 15 – 20 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Number 5,638,367 ("*Gaytan*"), in view of U.S. Patent Number 6,023,738 ("*Priem*"), and further in view of U.S. Publication Number 20040213291 ("*Beshi*"). Applicants respectfully traverse this rejection for at least the reason that *Gaytan* in view of *Priem* and *Beshi* fails to disclose, teach, or suggest all of the elements of claims 2 – 4, 6 – 13, and 15 – 20. More specifically, dependent claims 2 – 4 are allowable for at least the reason that these claims depend from and include the elements of allowable independent claim 1. Dependent claims 6 – 13 are allowable for at least the reason that these claims depend from and include the elements of allowable independent claim 5. Further, dependent claims 15 – 20 are allowable for at least the reason that they depend from and include the elements of allowable independent claim 14. *In re Fine*, *Minnesota Mining and Mfg.Co. v. Chemque, Inc.*, 303 F.3d 1294, 1299 (Fed. Cir. 2002).

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested.

Any other statements in the Office Action that are not explicitly addressed herein are not intended to be admitted. In addition, any and all findings of inherency are traversed as not having been shown to be necessarily present. Furthermore, any and all findings of well-known art and Official Notice, or statements interpreted similarly, should not be considered well-known for the particular and specific reasons that the claimed combinations are too complex to support such conclusions and because the Office Action does not include specific findings predicated on sound technical and scientific reasoning to support such conclusions.

If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

/afb/
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